CLAIMS

1. A reproduction signal processor comprising:

an analog/digital converter for sampling an analog signal, and converting the same into the digital signal;

an automatic equalizer for performing an automatic equalization of the digital signal;

a phase locked loop for generating a reference clock which coincides with a phase included in the digital signal and reference frequency components; and

a frequency divider for generating a frequency-divided clock obtained by performing integral multiplication of the period of the reference clock, and outputting the frequency-divided clock as an operation clock to the analog/digital converter and the automatic equalizer, wherein

the automatic equalizer is composed of:

a transversal filter for performing waveform equalization of the digital signal;

a straight-line interpolation unit for interpolating the omission of the sampling number due to the sampling using the frequency-divided clock in the output of the transversal filter; and

a control unit for estimating an equalization target value in accordance with the output of the transversal filter, and controlling a parameter of the transversal filter such that an

equalization error which is an error between the equalization target value and the output of the transversal filter becomes minimum.

2. The reproduction signal processor of Claim 1 wherein the straight-line interpolation unit is composed of:

a flip-flop element for performing a delay processing of an output equalization signal of the transversal filter for one period of the frequency-divided clock; and

an adder for adding a signal after the delay processing and the output equalization signal.

3. The reproduction signal processor of Claim 1 wherein,

instead of the straight-line interpolation unit, a high-order interpolation unit for interpolating the omission of the sampling number due to the sampling using the frequency-divided clock in the output of the transversal filter is provided.

4. The reproduction signal processor of Claim 3 wherein the high-order interpolation unit is composed of:

a flip-flop element for performing delay processing for one period of the frequency-divided clock;

plural multipliers for performing weighting of a tap coefficient on a signal after the delay processing; and

an adder for adding an output signal of the plural multipliers.